Team sdmay22-14

Project Title: RISC-V SoC Hardware Vulnerability Detection Toolset

Date: 10/31/2021

Members:

- Mason Korkowski -

- Micah Mundy -

- Gerald Edeh -

- Kolton Keller -

-Eva Kohl -

- Savva Zeglin -

- Magnus Anderson -

What we've accomplished in the past week/what we've been researching

- Mason Korkowski - Installed 2018 SoC design on the team server. Worked on pulling a specific file to test the linter. Finished getting the linter up and running. It is able to parse and detect errors in basic verilog examples.

- Micah Mundy - Worked with Magnus to simulate the 2018 Hack@DAC SoC RTL.

- Gerald Edeh - Discussed with team on how to get the 2018 SoC running. Also presented lightning talk as well.

- Kolton Keller - Trying out simulating the 2021 SoC on HPC clusters. Determining if program compilation or SoC startup takes a very long time.

-Eva Kohl - Worked on finding/ creating component diagrams of the of the SoC chip design using various softwares and participated in weekly meetings.

- Savva Zeglin - Generally further researched and tried to understand bugs

- Magnus Anderson - Worked on getting the 2018 Hack@Dac running on Coover computers - was stymied by missing software. Participated in presenting the project design in-class.

What we're planning to do in the coming week

- Mason Korkowski - Continue trying to find the incomplete base case bug using the linter. If the linter in its current state can find this bug then the proof of concept for static analysis is complete.

- Micah Mundy - Simulate the 2018 RTL or die trying

- Gerald Edeh - Continue to research, and work on YouTube assignment due next week

- Kolton Keller - Attempt to get one sudo command run on the HPC clusters and ask for more space if the team determines that moving forward is worthwhile.

-Eva Kohl - Continue to explore diagram software and learn verilog coding.

- Savva Zeglin - Attempt to use 2018 Hack@Dac SoC and look into a prototype for a tool that could find basic bugs (e.g. memory aliasing when there shouldn't be)

- Magnus Anderson - Finish getting the 2018 build running on a machine which has root access; hopefully also finish it on a machine with QuestaSim Installed.

Issues we had in the previous week

- Mason Korkowski - 2018 design is very difficult to actually install. It required 4 separate Repos, Sudo access, and a lot of time. This caused headaches because of the inability to install it on the default linux computers in the labs.

- Micah Mundy - Right now, we're trapped with two options that don't work. We've tried installing the dependencies for running the SoC on our computers and VMs, but one important dependency is licensed, closed-source software (Questasim). We've also tried using the 381 lab computers (with Questasim licenses), but the operating system and software on these devices is ancient, and they are heavily locked down.

- Gerald Edeh - There was an issue with running the 2018 SoC this past week

- Kolton Keller - Running the 2021 SoC on HPC clusters requires sudo access, which we do not have. Also, the max size of a personal folder in the clusters is 5 GB, and the SoC is easily over double that size.

-Eva Kohl - I'm not familiar with the simulation software used in running the SoC chip design and so that's been a learning curve.

- Savva Zeglin - Generally did not have time to get as much done as I wanted

- Magnus Anderson - The RHEL computers in the labs have ancient versions of software or common development tools not even installed.